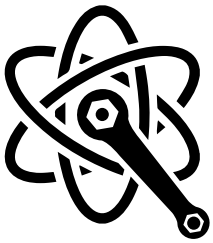

ARTIQ
Status report

August 2nd, 2017

1 NU-Servo

The Novogorny-Urukul-Servo (NU-Servo) is an initial design of a integrated combination of multichannel analog-to-digital converter (ADC, Novogorny), proportional-integral controller (FPGA, Kasli), and direct digital synthesizer (DDS, Urukul). It will become a dedicated mode of operation for Novogorny/Kasli/Urukul that can be used to implement flexible intensity stabilization schemes tailored to AOM-controlled laser beams directly feeding back onto the amplitude scale factor of the DDS. It is highly pipelined and resource saving using only a single multiplier while still supporting 8 channels and 32 independent profiles per channel. We plan to support sample rates of around 1 MHz and analog-to-analog latencies (through ADC, FPGA, DDS) of 1-2 Âţs. We are currently developing it in its own repository (`https://github.com/m-labs/nu-servo`). The work is funded by the team at the University of Oxford.

2 Sinara hardware

2.1 Manufacturing

DAC (Zotino) and ADC (low-speed Novogorny) modules work, and are ready for integration with ARTIQ. They are currently being shipped to M-Labs. AC performance will be tested soon.

BNC and RJ45 boards and VHDCI breakouts are in production.

8 Sayma AMC have been produced and are currently under testing.

Production of the remaining Sayma RTM boards is still pending tests of the JESD204 DACs on the first prototype.

2.2 DDR3 on Sayma

Both the 32-bit and the 64-bit DDR3 memories on Sayma have been successfully tested with the PHY we have developed and our controller.

2.3 Sayma AMC-RTM Wishbone bridge

The serial Wishbone link between the Sayma AMC and RTM cards is now operational and will be used to configure clocking chips, DACs and other non-realtime features of the RTM card from the AMC.

2.4 Sayma clocking and DAC testing

Very preliminary configuration of the HMC830 and the HMC7043 is done. DAC0 and DAC1 are responding to SPI, but there are currently some issues with the JESD high-speed interface, which are being investigated.

2.5 Sinara OpenOCD support

To implement smooth programming support and development tools for the Metlino/Sayma Ultrascale and Artix FPGAs we are extending OpenOCD to support those boards, the integrated programmers and FPGA chips. `https://github.com/m-labs/openocd`

3 ARTIQ software and generic gateware

3.1 ARTIQ 3.0 release plan

All the features in ARTIQ 3.0 have landed and the only item blocking the release is the fixing of TCP/IP stack problems. You can already test the 3.0 features by using the conda packages in our `dev` channel.

SAWG and DRTIO are part of ARTIQ-3 as "preview" features, and will be fully developed with Sinara support in ARTIQ-4.

3.2 Multi-satellite DRTIO

DRTIO masters now support multiple satellites. This is in a preliminary stage, and has received only limited testing because of the unavailability of Sinara hardware and the lack of an alternative multi-channel DRTIO-capable system that would not require significant investment.

3.3 Core device logging

The logs of the core device are now sent to the master (and the dashboard). This requires the use of a new controller, `aqctl_corelog`. The example environment (`artiq/examples/master`) automatically starts this controller when using `artiq_session`.

This logging mechanism is useful in particular to report RTIO collisions (which are now asynchronous with ARTIQ-3) and various DRTIO status reports and errors.

3.4 SAWG

The smart arbitrary waveform generator (SAWG) documentation has ben refined and extended. We have started investigating scalable ways to implement independent offsets/scale factors on the RTIO channels and taps to inject offsets/scale factors from gateware.

4 PDQ

To both streamline the PDQ development and to demonstrate how to develop out-of-tree code for ARTIQ we have move the PDQ components out of the ARTIQ repository into the main PDQ repository which now contains gateware, protocols, host side code for USB, ARTIQ code for SPI and documentation in one repository. `https://github.com/m-labs/pdq`