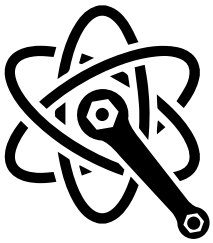

ARTIQ
Status report

September 5th, 2017

1 General ARTIQ software

1.1 ARTIQ manifesto

We have added a few paragraphs to the ARTIQ documentation explaining the practical aspects of using LGPLv3+ as the license for ARTIQ. `https://github.com/m-labs/artiq#the-artiq-manifesto`

1.2 ARTIQ-3 TCP/IP bug fixing

Some of the core device TCP/IP issues with ARTIQ-3 have been resolved. Updated packages for your testing are available in our conda `dev` channel.

1.3 Unit testing

`artiq_compile` and `artiq_rpctool` are now being run as part of the ARTIQ testing suite.

2 Sinara software and gateware support

2.1 Sayma target files

We have written ARTIQ target files for Sayma AMC and RTM, and have developed infrastructure so that configuration and status registers (CSRs) on the RTM FPGA appear as regular CSRs for the software on the AMC. This uses the Wishbone bridge transparently.

The code is available in the `sinara` branch of the ARTIQ repository.

2.2 Multiple JESD DAC support

We have modified the runtime and satellite manager so that they can initialize several JESD DAC chips (two on each Sayma).

2.3 RGMII Ethernet

We have rewritten the MiSoC RGMII PHY that was developed by Enjoy-Digital for Spartan-6 in order to make it cleaner and portable. We have integrated it into the Sayma MiSoC target, and are debugging it.

2.4 Flashing

We have added support to OpenOCD's FPGA/JTAG2SPI driver to support multiple TAPs. We are currently working on debugging that on Sayma.

We have rewritten a large part of `artiq_flash` to support Sayma.

3 Hardware

3.1 Sayma testing

We are able to generate correct clocks using the HMC830 and HMC7043. However, the DACs are not operating as some of the JESD lanes are problematic. We are still investigating.

3.2 Zotino testing

We are currently developing a test for the Zotino DAC card using the KC705, FMC DIO and VHDCI carrier.

3.3 Production update

The first production batch of 3U BNC, RJ45, SMA and VHDCI boards will ship next week.

3.4 Kasli and Urukul

The final changes to the schematics are being implemented and board layout has begun.

3.5 Grabber

The CameraLink EEM design has been finalized and layout is completed. Manufacture is on hold until funding is arranged. `https://github.com/m-labs/sinara/wiki/Grabber`