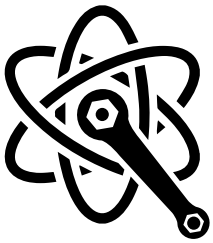

ARTIQ
Status report

March 5th, 2018

1 Sayma

1.1 Ethernet

We have investigated the packet transmission issues which boiled down to incorrect PHY chip settings and signal integrity issues that were corrected by changing the FPGA IOB settings.

To help with diagnostics, we have developed a low-level Ethernet analyzer (that can show the content of frames with broken preambles and FCS) and a traffic generator in gateware for Sayma. The code is at `http://github.com/m-labs/ethernet-yakshaving`.

We measured the RGMII TX timing window using the gateware and it matched what would be expected from the measurements on the hardware.

We are now able to use Ethernet reliably on one Sayma board. There are no packet losses and the results are reproducible between gateware builds. The rest of the ARTIQ stack (kernel loading etc.) also functions as expected.

Ethernet requires a board rework documented here: `https://github.com/m-labs/sinara/issues/484#issuecomment-360515298`

1.2 DDR3 SDRAM

Intermittent DDR3 problems have been found to manifest themselves on some boards and are being investigated. While looking into the problem, we improved the clocking of the IOSERDES in the gateware, but this did not have a significant effect on the issue.

1.3 Boot time

The bitstream loading during device boot in Sayma (and Kasli) has been accelerated by more than an order of magnitude.

2 Kasli

Multiple different Kasli gateware variants are in use in various laboratories. Kasli/v1.1 has been manufactured and has seen preliminary testing.

We have continued to develop tooling for the I2C tree on Kasli and the attached EEMs bypassing the FPGA. This enables easy EEM EEPROM commissioning and debugging of hardware on the I2C bus. A layout for the Sinara EEPROM data has been outlined.

We have also implemented commissioning of the FT4232H EEPROM that defines the Kasli USB interface. This permits vendors to embed serial numbers and enables global identification of Kaslis.

3 Urukul

Revision v1.1 of both Urukul variants has been manufactured and Urukul-AD9910/v1.1 has been tested successfully with Kasli and ARTIQ. We expect more than 30 Urukul boards to be in use in various laboratories soon.

We have released a new Urukul CPLD version implementing automatic latching of the shifted attenuator register settings on completion of the transfer and automatic loading of the status/configuration register at the beginning/end of a SPI transaction.

A new CPLD code pre-release targeting the changes in Urukul/v1.1 has been published.

4 Novogorny

The legacy 8 channel SPI ADC has received a complete ARTIQ core device driver interface. The driver was used to confirm specifications, and functionality of the design approach and is the basis for the upcoming Sampler driver. Novogorny is a legacy design and is expected to be outperformed and superseded by Sampler.

5 Other hardware

The Zotino and Grabber boards have arrived and are being tested.

The Thermostat schematics and initial PCB placement are done.

The BNC to IDC and HD68 to IDC adapters are now available and kept on stock.

6 DRTIO

We have completed the GTP transceiver implementation (Artix-7, Kasli) and added support for multiple master links.

We have optimized the RTIO core timing so that Kasli can use a 150MHz RTIO frequency, which makes it compatible with the 3Gbps DRTIO line rate used in Sayma/Metlino.

We have added APIs (`RTIOLinkError` and `get_drtio_link_status`) to handle links being down, in particular when using startup kernels.

We found issues with the Si5324 phase determinism and wander, that cause poor clock synchronization and data corruption. With helpful testing and suggestions by Chris Ballance and Thomas Harty, we designed a gateware- and software-based solution that will soon be implemented and tested.

7 SPI core

A new MiSoC SPI core has been written that resolves several design issues in the old SPI core. It has simpler clock divider programming and usage, better defined output signal buffering and registering, and a programming interface that is much easier to use, especially in the case of compound SPI transactions that consist of multiple transfers. All in-tree ARTIQ drivers have been ported. The out-of-tree PDQ SPI coredevice driver was ported as well.

8 Other ARTIQ software and gateware

We changed the layout of gateware build trees to make it easier to compile several gateware/firmware variants.

We fixed a race condition in the Ethernet core that resulted in intermittent core device panics.

We simplified the conda package definitions such that they are generic over the ARTIQ target and variant.

We ported an existing Princeton Instruments PICam library binding to Python 3, and implemented wrappers and workarounds required to use PICam on Linux.