ARTIQ
Status report

May 6th, 2018

1 Sayma debugging

1.1 HMC7043 noise

We discovered that before it is initialized, the HMC7043 generates broadband noise with components up to 2GHz, that caused random malfunction throughout the FPGA (including in parts of the design not clocked by the HMC7043). We found a workaround that consists in disabling the relevant FPGA input buffer until HMC7043 initialization.

Since the fixing of this bug, Sayma has been behaving in a much saner way than ever before.

1.2 HMC830

The HMC830 issue was due to the HMC7043 noise and has been resolved. The Sayma can now be clocked as intended from its 100MHz front panel input.

1.3 JESD204

We fixed the problem that caused intermittent initialization failures of the JESD204 links.

1.4 serwb

We improved the clocking of serwb, fixed a few bugs, and added bidirectional PRBS tests that are run at every initialization of the links to quickly identify data corruption issues.

1.5 1.8V bug

We have not observed 1.8V failures since the Exar firmware update; however, considering the rarity and random nature of this bug, this needs further testing before we can conclude that the problem is resolved.

1.6   Conclusion

Since the resolution of those issues and in particular the HMC7043 problem, Sayma has been behaving, in our tests, in a reliable manner. The tests included several dozens reboots (to RF output) of one board, during which no malfunction was observed. We believe it is now beginning to be usable for physics experiments.

2   SUServo

The Sampler-Urukul Servo connects the 8 channel ADC EEM (Sampler) with two 4 channel DDS EEMs (Urukul-AD9910) to form a versatile laser intensity stabilization system. It uses very few resources (2 BRAM, 1 DSP) while still providing low latency and high sample rate (1 MS/s). Among its features are support for 8 channels and 32 profiles per channel, RTIO-controlled profile/integrator/RF switch control, integrator hold, automatic integrator hold-off, and flexible ADC routing.

    The SUServo gateware is now fully integrated into ARTIQ and a basic coredevice driver is available. The DDS interface, and the IIR filter have been tested and the timing of the ADC confirmed. Integration testing and completion of the driver are ongoing.

3   picam

The out-of-tree driver for the Princeton Instruments EMCCD camera is functionally complete and has been tested. `https://github.com/quartiq/picam`

4   Sayma JESD204 synchronization

We are now controlling the phase of SYSREF using the HMC7043 and the DACs are responding in the expected manner (as reported by their status registers). We believe that they should be synchronized with each other when the phase is set to an appropriate value; we still need to observe the results at the DAC outputs.

5   AD9914 DDS high-resolution support

We have developed proof-of-concept code that extends the FTW of the AD9914 to 63 bits, by using the programmable modulus mode.

6   Sampling profiler

We have implemented a sampling profiler on the communications CPU, to help investigate core device performance issues. Profiling kernels and call graph construction support are not implemented at the moment.

7   Miscellaneous

We fixed several compiler crashes and miscompilations (#961, #974, #987). We upgraded LLVM to 6.0.0 and Rust to 1.25.0.

    We fixed race conditions on the core device affecting aqctl_corelog (#979) and rapid sequences of asynchronous RPCs (#985).

    We fixed issues in ARTIQ-4 with RTIO SED event replacement (#978).

    For the purpose of evaluating different CPU architectures and implementations, MiSoC now supports the VexRiscv RISC-V softcore CPU.