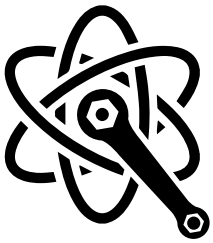

ARTIQ
Status report

August 9th, 2018

1 Sayma

1.1 DAC synchronization

The synchronization issues on a single Sayma were due to problems with HMC7043 configuration quirks combined with poorly documented HMC7043 silicon bugs, as well as the HMC7043 not being able to output a truly glitchless signal when modifying several delays at once. We have reworked the synchronization system to cope with these issues; and we no longer observe any DAC synchronization failures on a single board, with many reboots.

Synchronization across Sayma boards still does not work reliably. We have found that a major source of problems comes from the HMC7043 cycle slip feature, which is required by the inter-board synchronization mechanism, and causes obscure bugs when used.

1.2 Automatic SYSREF calibration

We have developed firmware that automatically determines working SYSREF phases for both the FPGA and the DACs and store them into the flash memory.

This removes the need for determining values manually by trial-and-error and writing them into the firmware code. This was particularly tedious as the FPGA value varies across boards and bitstream rebuilds due to Ultrascale process variations and poor I/O timing predictability originating from the Vivado router.

1.3 EEM support

We have developed and successfully tested code to use the EEM cards on Sayma with the VHDCI carrier board and a FMC to VHDCI card.

See: `artiq/examples/sayma_master/repository/demo.py`

1.4 JESD204 GTP_CLK2 issue

It remains poorly understood why some boards have problems with JESD204 when using the `GTP_CLK2` clock (a symptom of this bug is a failing PRBS test). To work around this problem in the meantime, we have modified the ARTIQ clocking structure so that it only uses `GTP_CLK1` at all times on all variants.

2 Grabber

The digital camera frame grabber and processing stack comprising the Grabber hardware EEM, gateware, firmware, and ARTIQ Python interfaces is completed and functional. It is being used in experiments.

3 Compiler bugfixing

We have fixed a few minor issues with the ARTIQ-Python compiler.

4 ARTIQ Docker images

As part of the opticlock project we have designed automatic infrastructure to build Docker images of ARTIQ environments. We plan to use them for automatic testing with hardware in the loop as part of continuous integration similar to what we are already doing with the M-Labs buildbot as well as for actual automated deployments of ARTIQ.

The images are currently not designed to be used for exposing the graphical user interface or for ARTIQ or experiment development.

`https://hub.docker.com/r/quartiq/artiq/`

5 Mirny

An initial version of the schematics for the Mirny microwave synthesizer EEM is available for review and discussions.

`https://github.com/sinara-hw/mirny`