BWRC iBob jumper settings

2007jul24 MRD 2006dec28 created; revised to include D MacMahon's DDC related functions
2007may31 add in phase switch and TCP/IP address functions.
2007jul23 add in the multi-colored shunts for the MAC ID and TCP/IP
2007jul24 add in examples of TCP/IP and Mac ID addresses (J8 jumpers)

notes **default** settings are in **bold**
All shunts are black unless otherwise designated

Jumper	**pins**	**Pitch**	**size**	**Vendor**	**Part number**	**Shunt to use**	**signal name or function**	**shunt installed shorted pins**	**shunt gone not connected**	**notes**
J1	1, 2	0.1"	1 x 2	Samtec	TSW_102_26_G_S	SNT_100_BK_G	PROG_ (active low)	Program the FPGA	**FPGA operational**	in parallel with the push button switch SW1
J2	1, 2	0.1"	1 x 2	Samtec	TSW_102_26_G_S	SNT_100_BK_G	VCC1_5 to VCCO_BANK01	VCCO_BANK01 is set to 1.5V	**VCCO_BANK01 is set by other J3,J4 or J5**	
J3	1, 2	0.1"	1 x 2	Samtec	TSW_102_26_G_S	SNT_100_BK_G	VCC1_8 to VCCO_BANK01	VCCO_BANK01 is set to 1.8V	**VCCO_BANK01 is set by other J2,J4 or J5**	
J4	1, 2	0.1"	1 x 2	Samtec	TSW_102_26_G_S	SNT_100_BK_G	VCC2_5 to VCCO_BANK01	**VCCO_BANK01 is set to 2.5V; this is the default**	VCCO_BANK01 is set by other J2, J3 or J5	
J5	1, 2	0.1"	1 x 2	Samtec	TSW_102_26_G_S	SNT_100_BK_G	VCC3_3 to VCCO_BANK01	VCCO_BANK01 is set to 3.3V	**VCCO_BANK01 is set by other J2, J3 or J4**	
J7	See the connector page as not all J7 pins are defined for mode/configuration jumpers									
J7	5,6	0.1"	2 x 20	Samtec			GPIO1_2; Msbit walsh sel: input 0	Input 0 walsh select Msbit is a logic 1; unless overwritten by software	**Input 0 walsh select Msbit is a logic 0**	For all walsh select signals :
J7	3,4	0.1"	2 x 20	Samtec			GPIO1_1; midbit walsh sel: input 0	Input 0 walsh select midbit is a logic 1; unless overwritten by software	**Input 0 walsh select midbit is a logic 0**	Shunt installed shorts PCB signal to GND
J7	1,2	0.1"	2 x 20	Samtec			GPIO1_0; Lsbit walsh sel: input 0	Input 0 walsh select Lsbit is a logic 1; unless overwritten by software	**Input 0 walsh select Lsbit is a logic 0**	FPGA inverts signal so PCB 0V = logic 1.
J7	13,14	0.1"	2 x 20	Samtec			GPIO1_6; Msbit walsh sel: input 1	Input 1 walsh select Msbit is a logic 1; unless overwritten by software	**Input 1 walsh select Msbit is a logic 0**	May be overwritten by software
J7	11,12	0.1"	2 x 20	Samtec			GPIO1_5; midbit walsh sel: input 1	Input 1 walsh select midbit is a logic 1; unless overwritten by software	**Input 1 walsh select midbit is a logic 0**	
J7	9,10	0.1"	2 x 20	Samtec			GPIO1_4; Lsbit walsh sel: input 1	Input 1 walsh select Lsbit is a logic 1; unless overwritten by software	**Input 1 walsh select Lsbit is a logic 0**	
J7	21,22	0.1"	2 x 20	Samtec			GPIO1_10; Msbit walsh sel: input 2	Input 2 walsh select Msbit is a logic 1; unless overwritten by software	**Input 2 walsh select Msbit is a logic 0**	
J7	19,20	0.1"	2 x 20	Samtec			GPIO1_9; midbit walsh sel: input 2	Input 2 walsh select midbit is a logic 1; unless overwritten by software	**Input 2 walsh select midbit is a logic 0**	
J7	17,18	0.1"	2 x 20	Samtec			GPIO1_8; Lsbit walsh sel: input 2	Input 2 walsh select Lsbit is a logic 1; unless overwritten by software	**Input 2 walsh select Lsbit is a logic 0**	
J7	29,30	0.1"	2 x 20	Samtec			GPIO1_14; Msbit walsh sel: input 3	Input 3 walsh select Msbit is a logic 1; unless overwritten by software	**Input 3 walsh select Msbit is a logic 0**	
J7	27,28	0.1"	2 x 20	Samtec			GPIO1_13; midbit walsh sel: input 3	Input 3 walsh select midbit is a logic 1; unless overwritten by software	**Input 3 walsh select midbit is a logic 0**	
J7	25,26	0.1"	2 x 20	Samtec			GPIO1_12; Lsbit walsh sel: input 3	Input 3 walsh select Lsbit is a logic 1; unless overwritten by software	**Input 3 walsh select Lsbit is a logic 0**	
Walsh select = 0b111 =7 is the highest frequency walsh signal; walsh select = 0b000 = 0 is the slowest frequency walsh signal										
J7	33,34	0.1"	2 x 20	Samtec			GPIO1_16; walsh unswitch enable	Disable walsh phase Unswitching on all inputs	**Enable walsh phase unswitching (all inputs)**	
J8	See the connector page as not all J8 pins are defined for mode/configuration jumpers									
J8 1,2 thru 27, 28 are derived from the PCB, assembly run and serial numbers and are used to set the MAC ID and IP address										
MAC ID will be 00:6d:12:1b:AB:CD where AB:CD is 0b 1 0 BPIO2_13. BPIO2_12: BPIO2_11..8: BPIO2_7..4: BPIO2_3..0										
IP ID will be 169.254.AB.CD where AB:CD is 0b 1 0 BPIO2_13. BPIO2_12: BPIO2_11..8: BPIO2_7..4: BPIO2_3..0										
For all IP address bits:	Shunt installed shorts PCB signal to GND									
	FPGA inverts signal so PCB 0V = logic 1.									
J8	27,28	0.1 x 0.1"	2 x 20	Samtec	**These shunts are**	3/M 929953-30	GPIO2_13; Lsbit 13 of MAC & IP addr, r1	MAC, IP addr bit 13, r1 is a logic 1	**MAC, IP addr bit 13, r1 is a logic 0**	0br1r0 is the revision number of the PCB
J8	25,26	0.1 x 0.1"	2 x 20	Samtec	**Gray**	517-953-30	GPIO2_12; Lsbit 12 of MAC & IP addr, r0	MAC, IP addr bit 12, r0 is a logic 1	**MAC, IP addr bit 12, r0 is a logic 0**	And is 0..3
J8	23,24	0.1 x 0.1"	2 x 20	Samtec	**These shunts**	Mouser	GPIO2_11; Lsbit 11 of MAC & IP addr, a3	MAC, IP addr bit 11, a3 is a logic 1	**MAC, IP addr bit 11, a3 is a logic 0**	0ba3a2a1a0 is the assembly run number
To					**are**	151-8003				And is 0..15
J8	17,18	0.1 x 0.1"	2 x 20	Samtec	**Red**		GPIO2_8; Lsbit 8 of MAC & IP addr, a0	MAC, IP addr bit 8, a0 is a logic 1	**MAC, IP addr bit 8, a0 is a logic 0**	
J8	15,16	0.1 x 0.1"	2 x 20	Samtec	**These shunts**	Mouser	GPIO2_0; Lsbit 0 of MAC and IP addr, s7	MAC, IP addr bit 0, s7 is a logic 1	**MAC, IP addr bit 7, s7 is a logic 0**	0bs7s6s5s4s3s2s1s0 is the serial number of the
To					**are**	151-8001				Ibob and is 0..255
J8	1,2	0.1 x 0.1"	2 x 20	Samtec	**Blue**		GPIO2_0; Lsbit 0 of MAC and IP addr, s0	MAC, IP addr bit 0, s0 is a logic 1	**MAC, IP addr bit 0, s0 is a logic 0**	

Examples	iBob rev	Assembly Run	Serial Number	TCP/IP Address	rev;run;S/N	TCP/IP address	HCRO iBob "hardware" names (hcro.org suffix not shown)
					0; 1; N	169.254.129.N	ibob-aN
	1	1	39	169.254.145.39	1; 1; N	169.254.145.N	ibob-bN
	2	1	14	169.254.161.14	2; 1; N	169.254.161.N	ibob-cN
	2	2	7	169.254.162.7	2; 2; N	169.254.162.N	ibob-dN
	3	1	28	169.254.177.28	3; 1; N	169.254.177.N	ibob-eN
	3	2	11	169.254.178.11	3; 2; N	169.254.178.N	ibob-fN
	3	3	44	169.254.179.44	3; 3; N	169.254.179.N	ibob-gN

J10	1,2		0.1"x0.1"		2 x 8					SNT_100_BK_G		DIPSW_SIGS<0>		DIPSW_SIGS<0> is shorted to GND.		**DIPSW_SIGS<0> is pulled to 2.5V**					
J10	3,4									SNT_100_BK_G		DIPSW_SIGS<1>		DIPSW_SIGS<1> is shorted to GND.		**DIPSW_SIGS<1> is pulled to 2.5V**					
J10	5,6									SNT_100_BK_G		DIPSW_SIGS<2>		DIPSW_SIGS<2> is shorted to GND.		**DIPSW_SIGS<2> is pulled to 2.5V**					
J10	7,8									SNT_100_BK_G		DIPSW_SIGS<3>		DIPSW_SIGS<3> is shorted to GND.		**DIPSW_SIGS<3> is pulled to 2.5V**					
J10	9,10									SNT_100_BK_G		DIPSW_SIGS<4>		DIPSW_SIGS<4> is shorted to GND.		**DIPSW_SIGS<4> is pulled to 2.5V**					
J10	11,12									SNT_100_BK_G		DIPSW_SIGS<5>		DIPSW_SIGS<5> is shorted to GND.		**DIPSW_SIGS<5> is pulled to 2.5V**					
J10	13,14									SNT_100_BK_G		DIPSW_SIGS<6>		DIPSW_SIGS<6> is shorted to GND.		**DIPSW_SIGS<6> is pulled to 2.5V**					
J10	15,16									SNT_100_BK_G		DIPSW_SIGS<7>		DIPSW_SIGS<7> is shorted to GND.		**DIPSW_SIGS<7> is pulled to 2.5V**					
J11	1,2		0.1"		1 x 3			SIP 1x3		SNT_100_BK_G		MGT_BOTTOM_CLK_M		XTAL2 125.00 Mhz; note many boards do NOT have 125MHz XTALs		pin 2 must be				J11 and J12 shunts must be in same position!	
J12	1,2		0.1"		1 x 3			SIP 1x3		SNT_100_BK_G		MGT_BOTTOM_CLK_P		XTAL2 125.00 Mhz; installed and thus this mode may be nonfunctional.		tied to pin 1 or				pin 3s are labled	
J11	2,3		0.1"		1 x 3			SIP 1x3		SNT_100_BK_G		MGT_BOTTOM_CLK_M		**XTAL3 156.25 Mhz**; many boards only have 156.25 Mhz XTALs		pin 2 must be				J11 and J12 shunts must be in same position!	
J12	2,3		0.1"		1 x 3			SIP 1x3		SNT_100_BK_G		MGT_BOTTOM_CLK_P		**XTAL3 156.25 Mhz;**thus jumpers must be in these positions		tied to pin 3 (or pin 1 shown above)				pin 3s are labled	
J13	1,2		0.1"		1 x 3			SIP 1x3		SNT_100_BK_G		MGT_TOP_CLK_M		XTAL2 125.00 Mhz; note many boards do NOT have 125MHz XTALs		pin 2 must be				J13 and J14 shunts must be in same position!	
J14	1,2		0.1"		1 x 3			SIP 1x3		SNT_100_BK_G		MGT_TOP_CLK_P		XTAL2 125.00 Mhz; installed and thus this mode may be nonfunctional.		tied to pin 1 or				pin 3s are labled	
J13	2,3		0.1"		1 x 3			SIP 1x3		SNT_100_BK_G		MGT_TOP_CLK_M		**XTAL3 156.25 Mhz**; many boards only have 156.25 Mhz XTALs		pin 2 must be				J13 and J14 shunts must be in same position!	
J14	2,3		0.1"		1 x 3			SIP 1x3		SNT_100_BK_G		MGT_TOP_CLK_P		**XTAL3 156.25 Mhz;**thus jumpers must be in these positions		tied to pin 3 (or pin 1 shown above)				pin 3s are labled	
J15	1,2		0.1" x 0.1"		2 x 3			SIP 2x3		SNT_100_BK_G		FPGA_CFGMODE0; U1.AF26		M0 = 0		**M0 = 1**				See table below	
J15	3,4									SNT_100_BK_G		FPGA_CFGMODE1;U1.AE26		M1 = 0		**M1 = 1**				See table below	
J15	5,6									SNT_100_BK_G		FPGA_CFGMODE2, U1.AE25		**M2 = 0**		M2 = 1				See table below	
	M2:M1:M0 = 0b110 = Slave SelectMap Mode. Virtex II Pro FPGA is programmed 8bits at a time from memory mapped writes over the cPCI bus. This is the DEFAULT.																						
	M2:M1:M0 = 0b111 = Slave Serial Mode. Virtex II Pro FPGA is programmed 1bit at a time from memory mapped writes over the cPCI bus (saves 7 pins over Slave Select Map).																						
	M2:M1:M0 = 0b101 = JTAG (boundary scan) programming; recommended for programming the PROM and is specified in the official iBob initial test procedure																						
	M2:M1:M0 = **0b011** = Master SelectMAP mode; **This is the default.** FPGA is the source of CCLK,DONE and INIT_B(to PROM's RESET_/OE)																						
J16	1,2		0.1" x 0.1"		2 x 3			SIP 2x3		SNT_100_BK_G		REV_SEL_MODE0: U2-25		design revision set by REV_SEL_MODE1:2 bits		**internal revision select control bits**				EN_EXT_SEL_ on the flash PROM	
J16	3,4									SNT_100_BK_G		REV_SEL_MODE1: U2-26		MODE[1:0] = select 1 of 4 unique designs stored within the 1 PROM IC		**ignored due to MODE0; do not install**				REV_SEL0 on the flash PROM	
J16	5,6									SNT_100_BK_G		REV_SEL_MODE2: U2-27		when enabled by REV_SEL_MODE0 shunt installed; otherwise ignored.		**ignored due to MODE0; do not install**				REV_SEL1 on the flash PROM	
	design revision set by REV_SEL_MODE1:2 bits																						
	MODE[1:0] = select 1 of 4 unique designs stored within the 1 PROM IC																						
	when enabled by REV_SEL_MODE0 shunt installed; otherwise they are ignored.																						

BWRC iBob jumper settings

2006dec28 MRD created

These aren't jumpers exactly but they are connectors and have Jxx reference designators.

Jumper	pins	Pitch	size	PCB conn. type	Connector Vendor	Connector Part number	signal name or function	Mating connector Vendor	Mating connector Part Number	notes
J6	1 to 40	0.1 x 0.1"	2 x 20	DIP 2 x 20			GPIO0_[0..19]			closest to the FPGA, pin 1 marked with "o"; all even pins=GND
J6	1,5,9,13,17,21,25,29						LVTTL; GPIO0_0,2,4,6,8,10,12,14 External sync out signals; for syncing standalone iBobs when no external sync signal is available.			
J7	1 to 40	0.1 x 0.1"	2 x 20	DIP 2 x 20			GPIO1_[0..19]			just closer to PCB edge than J6, pin 1 marked with "o"; all even pins=GND
										See the Jumper page as well; part of J7 is used for mode/config jumpers
J8	1 to 40	0.1 x 0.1"	2 x 20	DIP 2 x 20			GPIO2_[0..19]			closest to PCB edge, pin 1 marked with "o"; all even pins=GND
										See the Jumper page as well; part of J8 is used for mode/config jumpers
J9	1 to 40	0.1 x 0.1"	2 x 20	DIP 2 x 20			GPIO3_[0..19]			just farther from PCB edge than J8, pin 1 marked with "o"; all even pins=GND
J9	33						LVTTL; GPIO3_16; Walsh output for input 0; for monitoring or driving level shifters/mixers etc			
J9	35						LVTTL; GPIO3_17; Walsh output for input 1; for monitoring or driving level shifters/mixers etc			
J9	37						LVTTL; GPIO3_18; Walsh output for input 2; for monitoring or driving level shifters/mixers etc			
J9	39						LVTTL; GPIO3_19; Walsh output for input 3; for monitoring or driving level shifters/mixers etc			
D11	1 to 2	0.1"	1 x 2	SIP 1 x 2	Samtec	TSW_102_26_G_S	+5VDC for fan	Molex	08-50-0114	two (2) KK-Series female 22-30AWG crimp terminals
								Molex	22-01-3037	KK-series 3-pin housing
J17	1 to 9	0.1"	1 x 9	SIP 1 x 9	Samtec	TSW_109_14_G_S	JTAG			VCC2_5, GND, NC, JTAG_TCK, NC, JTAG_TDO, JTAG_TDI, NC, JTAG_TMS
J18	1 to 5	0.1"	1 x 5	sip 1 x 5			RS232 link			RS232 RX,TX,GND,CTS, RTS
J19	1 to 2			50A Power	Molex	42820-2212	VCC5	Molex	42815-0011	two (2) 10 AWG Mini-Fit Sr. power cable crimp terminals
								Molex	42816-0212	2-pos Mini-Fit Sr power cable housing
J20	1 to 25			INFINIBAND 4X	Molex	91804-0410	Top infiniband link 0			also has 6 mounting pins; this connector gets screwed to the PCB
J21	1 to 25			INFINIBAND 4X	Molex	91804-0410	bottom infiniband link 1			also has 6 mounting pins; this connector gets screwed to the PCB
J22	1 to 144			40-PAIR LVDS Z-DOK+ Host	Tyco	6367550-5	ADC0 diff. inputs			J22 is closer to the 100 Mbit connector
J23	1 to 144			40-PAIR LVDS Z-DOK+ Host	Tyco	6367550-5	ADC1 diff inputs			J23 is closer to the VDC input power connector
J24	1 to 80		MDR	80-PIN MINI D RIBBON RA	3M	N10280-52E2VC	LVDS_GPIO_M/P[0..39]			
J115	1 to 12	.072"	RJ45	MAGJACK SMT 10/100Mbit with LEDs	Pulse	J3011G21D	PHY_TPO, TPI, LAN_LED, …	CAT-5e, … cable		only available on v1_rev2 and v1_rev3 boards; some of the v1_rev2 iBobs have faults that cause Ethernet failures