This is the ALPHA 0 version of the GUPPi Output FPGA (FPGA2)

MODIFIED: 07-JUL-08 by -RLM- to add packed registers in all control and data pipes as noted below...

NOTES:

1) All Inter-FPGA Data and Control Pipes are now implemented WITH packed registers and incorporate PULLUP terminations.

2) All out-going pipes (in U1, U2, and U3) have packed registers with Phase Delay = 0 and PULLUPs

3) In-coming pipes involving U1 (in either direction) have packed registers with Phase Delay = 180 and PULLUPs; and are followed by a delay block having Z = -(N+1) (i.e., one extra clock cycle delay)

4) In-coming pipes involving U3 (in either direction) have packed registers with Phase Delay = 0 and PULLUPs; and are followed by a delay block having Z = -(N) (i.e., no extra clock cycle delay)

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Data Pipes 0 and 1, in-coming from U3 have packed registers with Phase Delay =180 and PULLUPs; and are followed by a delay block having Z = -(N+1) (i.e., one extra clock cycle delay)

07-JUL-08
-RLM-

5) The above mentioned extra clock cycle delay for the U3 Data Pipes have been removed. All U3 Data Pipe delays are Z^-3.rr

22-OCT-08
- RLM, JMR -

6) New BW adjustment blocks have been added to U3's Data Pipes to accomodate the various IOB delays required to implement BWs of 200MHz, 400MHz, and 800MHz. A software reg. named "BW_SEL" was added to allow selection of BW as follows...

0 = 200MHz, 1 = 400MHz, 2 = 800MHz

23-OCT-08
-RLM-

This version has the following changes

1) The bit packer has been modified appropriately (based on simulation) to accomodate a one clock delay between the BRAM address and the BRAM data out. This was causing a 4-bin offset in the spectrum. This mod was basically to have two versions of the address counter, one version delayed by one clock.

2) There is a custom time division demux block which outputs the data in the order required. The asynchronous nature of the xilinx time division demux block was causing the bins to intermittently shift by +4 positions after each "arm", depending on whether the "arm" happened on an odd or even system clock cycle.

3) All of the counters' reset inputs have been modified to accomodate the requirement that they be enabled during a reset pulse.

4) The Z^-3 delays between the vacc's and the bit packer were removed. They were causing a 16-bin offset in the spectrum.

14-AUG-08
- JMR -

5) Latencies were added within the Stokes blocks to alleviate timing errors and possibly fix erratic results observed in "V"

19-AUG-08
-RLM-

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6) Modified calculations for I, Q, U, & V to correct problems with U & V

20-AUG-08
-RLM

7) Moved distributed delays into corresponding subsystems throughout

8) Changed re-interpret (cast) outputs to "Round +/- Inf" and changed those following Stokes blocks to 33_29 (to match other Stokes outputs

9) Sliced Accumulator Length down to 16 bits and reduced width of corresponding constant "1s" inside Disintegrator subsystems

23-SEP-08
-RLM-

10) Changed re-interpret (cast) outputs back to "truncate" and eliminated latencies added by JMR (regression to earlier version; since the newer version wouldn't build without significant timing errors) and reverted to CASPER Power blocks within Stokes subsystems

26-SEP-08
-RLM-

11) Added Master Sync reset to counter in stage between packer and 10Ge manager to fix problem where async arm()'s would get (I&Q) & (U&V) streams interchanged.

28-OCT-08
-RLM-

12) Created a "Pipes_Capture_Subsystem" to clean up drawing

29-OCT-08
-RLM-