OpenRISC Processor

Muhammadreza Haghiri

Who am I?

I'm Muhammadreza Hagiri, student of Computer Hardware engineering , Islamic Azad University Central Tehran Branch (IAUCTB)

You can contact me on twitter :
http://twitter.com/prpe26

And also telegram :

http://telegram.me/Haghiri75

And visit my blog :

http://haghiri75.com

What's OpenRISC?

OpenRISC is an attempt to develop a *free instruction set architecture* by idea of RISC.

It's the original flagship of the OpenCores community.

It's published under GNU Lesser General Public License (LGPL), and the firmware is published under GNU General Public License (GPL)

What's RISC?

RISC stands for *Reduced Instruction Set Computer* and it means a little instruction set architecture, with benefit of higher speed in operations.

The main feature of RISC is huge number of registers, one-cycled execution time and pipelining.

OpenRISC instruction set

- 16 or 32 registers
- 3-operand load – store architecture (MIPS-like)
- Fixed 32 bit instruction length
- Includes all features of modern server/desktop processors.

Operating System

- **Linux**
- **RTOS (Real Time Operating System)**

The Machine Code

There are 10 kind of instructions :

I. Class I (Must be always implemented)

II. Class II

The Machine Code

Example :

RD [31:0] = Operation(RA[31:0], RB[31:0])

add rD, rA, rB

xor rD, rA, rB

It’s all MIPS-like!

Implementation

It's a free and open source HDL code, you can download it from : http://openrisc.github.io

Then, you need to compile the code on FPGA boards, to make your very own OpenRISC processor.

Similar projects

- OpenSPARC
- RISC-V
- lowRISC
- LadyBug (my own project)
- And a lot of others ...

Thanks for watching!