Re: can M5 simulator act as CMP/SMP simulator?
2005-10-31 05:27

```
Sorry for not replying to your earlier message.  I had to clarify
exactly where we're at with MP simulation.  Right now you can simulat
multiple processors on a coherent bus as long as (1) there is only on
bus that has multiple caches connected to it and (2) there is only on
level of cache above the shared bus.  That is, like this:

CPU --- L1 --|
             |--- MEM
CPU --- L1 --|

or like this:

CPU --- L1 --|
             |--- L2 --- MEM
CPU --- L1 --|

but NOT like this:

CPU --- L1 --- L2 --|
                    |--- MEM
CPU --- L1 --- L2 --|

If you want to do something more complicated you'll need to extend th
coherence protocol yourself.

Note that SMP vs CMP is only a matter of how you configure the
bandwidths and latencies; topologically they are not necessarily any
different.

The detailed CPU model also supports SMT, but Linux does not support
Alpha CPUs, so you won't be able tpo take advantage of SMT in
full-system mode without some kernel hacking.  It should work for
syscall emulation though.

Steve

xiao junhua wrote:
> I want to use M5 to simulate CMP architecture.
> can it do that function?
> I'm not sure. just use it for serval days.
>
> would anyone help me?
>
> _________________________________________________________________
>    ?[illegible]L?L[illegible] ?? MSN Hotmail??  http://www.hotmail.com
>
>
```

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can M5 simulator act as CMP/SMP simulator?	xiao junhua <xiao_401@ho...>	2005-10-31 02:22